INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
043876-0147	**10/705,946**
APPLICANT: **HANSEN, C., et al.**	
FILING DATE: **November 13, 2003**	GROUP: **2183**

U.S. PATENT DOCUMENTS

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Eric Coles	3/3/06

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. 043876-0147	SERIAL NO. 10/705,946
	APPLICANT HANSEN, C., et al.	
	FILING DATE November 13, 2003	GROUP 2183

EXAMINER'S INITIALS	CITE NO.	OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
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(Suppl.)INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
43876-147	**C ntinuati n f Serial No. 10/436,340**
APPLICANT: **Craig HANSEN, et al.**	
FILING DATE: **November 13, 2003**	GROUP: **To be assigned**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	1	of	10

Complete if Known	
Application Number	10/705,946
Filing Date	November 13, 2003
First Named Inventor	Craig C. HANSEN, et al.
Group Art Unit	2183
Examiner Name	CHAN, EDDIE P
Attorney Docket Number	43876-147

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EC	AT	WO 93/11500				

Examiner Signature	Eric Coleman	Date Considered	3/3/06

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/705,946
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				First Named Inventor	Craig C. HANSEN, et al.
(use as many sheets as necessary)				Group Art Unit	2183
				Examiner Name	CHAN, EDDIE P
Sheet	2	of	10	Attorney Docket Number	43876-147

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
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	CR	Knapp et al., "Bulk Storage Applications in the ILLIAC IV System," ILLIAC IV Document No. 250, Center for Advanced Computation, University of Illinois at Urbana-Champaign (August 3, 1971) (51056DOC001647 – 656)	
	CS	Awaga et al., "The μVP 64-bit Vector Coprocessor: A New Implementation of High-Performance Numerical Computation," IEEE Micro, Vol. 13, No. 5, pp. 24-36 (October 1993) (51056DOC011921 – 934)	
EC	CT	Takahashi et al., "A 289 MFLOPS Single Chip Vector Processing Unit," The Institute of Electronics, Information, and Communication Engineers Technical Research Report, pp. 17-22 (May 28, 1992) (51056DOC009798 – 812)	

Examiner Signature	Eric Chan	Dated Considered	3/3/06

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 5 of 10

Complete if Known	
Application Number	10/705,946
Filing Date	November 13, 2003
First Named Inventor	Craig C. HANSEN, et al.
Group Art Unit	2183
Examiner Name	CHAN, EDDIE P
Attorney Docket Number	43876-147

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
EC	CU	Uchiyama et al., "The Gmicro/500 Superscalar Microprocessor with Branch Buffers," IEEE Micro (October 1993) (51056DOC000185 – 194)	
	CV	Broughton et al., "The S-1 Project: Top-End Computer Systems for National Security Applications," (October 24, 1985) (51056DOC057368 – 607)	
	CW	Farmwald et al., "Signal Processing Aspects of the S-1 Multiprocessor Project," SPIE Vol. 241, Real-Time Signal Processing (1980) (51056DOC072280 - 291)	
	CX	Farmwald, "High Bandwidth Evaluation of Elementary Functions," IEEE Proceedings, 5th Symposium on Computer Arithmetic (1981) (51056DOC071029 -034)	
	CY	Gilbert, "An Investigation of the Partitioning of Algorithms Across an MIMD Computing System," (February 1980) (51056DOC072244 – 279)	
	CZ	Widdoes, "The S-1 Project: Developing High-Performance Digital Computers," IEEE Computer Society COMPCON Spring 1980 (December 11, 1979) (51056DOC071574 - 585)	
	DA	Cornell, S-1 Uniprocessor Architecture SMA-4 (51056DOC056505 - 895)	
	DB	The S-1 Project, January 1985, S-1 Technical Staff (51056DOC057368 – 607)	
	DC	S-1 Architecture and Assembler SMA-4 Manual, December 19, 1979 (Preliminary Version) (51056DOC057608 – 918)	
	DD	Michielse, "Performing the Convex Exemplar Series SPP System," Proceedings of Parallel Scientific Computing, First Intl Workshop, PARA '94, pp. 375-82 (June 20-23, 1994) (51056DOC020754 - 758)	
	DE	Wadleigh et al., "High Performance FFT Algorithms for the Convex C4/XA Supercomputer," Poster, Conference on Supercomputing, Washington, D.C. (November 1994) (51056DOC068618)	
	DF	C4 Technical Overview (September 23, 1993) (51056DOC017111 - 157)	
	DG	Saturn Assembly Level Performance Tuning Guide (January 1, 1994) (51056DOC017369 - 376)	
	DH	Saturn Differences from C Series (February 6, 1994) (51056DOC017150 - 157)	
	DI	"Convex Adds GaAs System," Electronic News (June 20, 1994) (51056DOC019388 - 390)	
	DJ	Convex Architecture Reference Manual, Sixth Edition (1992) (51056DOC016599 - 993)	
	DK	Convex Assembly Language Reference Manual, First Edition (December 1991) (51056DOC015996 - 6598)	
	DL	Convex Data Sheet C4/XA Systems, Convex Computer Corporation (51056DOC059235 - 236)	
	DM	Saturn Overview (November 12, 1993) (51056DOC017111 - 157)	
	DN	Convex Notebook containing various "Machine Descriptions" (51056DOC016994 – 7510)	
	DO	"Convex C4/XA Offer 1 GFLOPS from GaAs Uniprocessor," Computergram International, June 15, 1994 (51056DOC019383)	
	DP	Excerpt from Convex C4600 Assembly Language Manual, 1995 (51056DOC061441 – 443)	
	DQ	Excerpt from "Advanced Computer Architectures - A Design Space Approach," Chapter 14.8, "The Convex C4/XA System" (51056DOC061453 – 459)	
	DR	Convex C4600 Assembly Language Manual, First Edition, May 1995 (51056DOC064728 – 5299)	
EC	DS	Alvarez et al., "A 450MHz PowerPC Microprocessor with Enhanced Instruction Set and Copper Interconnect," ISSCC (February 1999) (51056DOC071393 - 394)	

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Sheet	6	of	10

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Application Number	10/705,946
Filing Date	November 13, 2003
First Named Inventor	Craig C. HANSEN, et al.
Group Art Unit	2183
Examiner Name	CHAN, EDDIE P
Attorney Docket Number	43876-147

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

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EC	DT	Tyler et al., "AltiVec™: Bringing Vector Technology to the PowerPC™ Processor Family," IEEE (February 1999) (51056DOC071035 - 042)	
	DU	AltiVec™ Technology Programming Environments Manual (1998) (51056DOC071043 - 392)	
	DV	Atkins, "Performance and the i860 Microprocessor," IEEE Micro, pp. 24-27, 72-78 (October 1991) (5156DOC070655 – 666)	
	DW	Grimes et al., "A New Processor with 3-D Graphics Capabilities," NCGA '89 Conference Proceedings Vol. I, pp. 275-84 (April 17-20, 1989) (5156DOC070711 – 717)	
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	EJ	Paragon User's Guide, Intel Corporation (October 1993) (51056DOC068802 – 9097)	
	EK	N15 Micro Architecture Specification, dated April 29, 1991 (50781DOC000001 - 982)	
	EL	N15 External Architecture Specification, dated October 17, 1990 (51056DOC017511 - 551)	
	EM	N15 External Architecture Specification, dated December 14, 1990 (50781DOC001442 - 509)	
	EN	N15 Product Requirements Document, dated December 21, 1990 (50781DOC001420 - 441)	
	EO	N15 Product Implementation Plan, dated December 21, 1990 (50781DOC001794 - 851)	
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Examiner Signature		Dated Considered	3/3/06

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Sheet	7	of	10

Complete if Known	
Application Number	10/705,946
Filing Date	November 13, 2003
First Named Inventor	Craig C. HANSEN, et al.
Group Art Unit	2183
Examiner Name	CHAN, EDDIE P
Attorney Docket Number	43876-147

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
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EC	ES	Arnould et al., "The Design of Nectar: A Network Backplane for Heterogeneous Multicomputers," ACM (1989) (51056DOC020947 – 958)	
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	EZ	Ghafoor, "Systolic Architecture for Finite Field Exponentiation," IEEE Proceedings, Vol. 136 (November 1989) (51056DOC071700 - 705)	
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	FE	Iwaki, "Architecture of a High Speed Reed-Solomon Decoder," IEEE Consumer Electronics (January 1994) (51056DOC071687 - 694)	
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	FG	Laudon et al., "Architectural and Implementation Tradeoffs in the Design of Multiple-Context Processors," Technical Report: CSL-TR-92-523 (May 1992) (51056DOC069301 – 327)	
	FH	Lawrie, "Access and Alignment of Data in an Array Processor," IEEE Transactions on Computers, Vol. C-24, No. 12, pp. 99-109 (December 1975) (51056DOC002932 – 942)	
	FI	Le-Ngoc, "A Gate-Array-Based Programmable Reed-Solomon Codec: Structure-Implementation-Applications," IEEE Military Communications (1990) (51056DOC071695 - 699)	
	FJ	Litzkow et al., "Condor – A Hunter of Idle Workstations," IEEE (1988) (51056DOC068712 – 719)	
	FK	Markstein, "Computation of Elementary Functions on the IBM RISC System/6000 Processor," IBM J. Res. Develop., Vol. 34, No. 1, pp 111-19 (January 1990) (51056DOC059620 – 628)	
	FL	Nienhaus, "A Fast Square Rooter Combining Algorithmic and Table Lookup Techniques," IEEE Proceedings Southeastcon, pp. 1103-05 (1989) (51056DOC061469 – 471)	
EC	FM	Renwick, "Building a Practical HIPPI LAN," IEEE, pp. 355-60 (1992) (51056DOC020937 – 942)	

Examiner Signature	Eric Chan	Dated Considered	3/3/06

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				Application Number	10/705,946
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	November 13, 2003
				First Named Inventor	Craig C. HANSEN, et al.
				Group Art Unit	2183
(use as many sheets as necessary)				Examiner Name	CHAN, EDDIE P
Sheet	8	of	10	Attorney Docket Number	43876-147

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EC	FN	Rohrbacher et al., "Image Processing with the Staran Parallel Computer," IEEE Computer, Vol. 10, No. 8, pp. 54-59 (August 1977) (reprinted version pp. 119-124) (51056DOC002943 – 948)	
	FO	Ryne, "Advanced Computers and Simulation," IEEE, pp. 3229-33 (1993) (51056DOC020883 – 887)	
	FP	Siegel, "Interconnection Networks for SIMD Machines," IEEE Computer, Vol. 12, No. 6 (June 1979) (reprinted version pp. 110 118) (51056DOC002949 – 957)	
	FQ	Singh et al., "A Programmable HIPPI Interface for a Graphics Supercomputer," ACM (1993) (51056DOC020888 – 896)	
	FR	Smith, "Cache Memories," Computing Surveys, Vol. 14, No. 3 (September 1982) (51056DOC071586 - 643)	
	FS	Tenbrink et al., "HIPPI: The First Standard for High-Performance Networking," Los Alamos Science (1994) (51056DOC020943 – 946)	
	FT	Tolmie, "Gigabit LAN Issues: HIPPI, Fibre Channel, or ATM," Los Alamos National Laboratory Report No. LA-UR 94-3994 (1994) (51056DOC046599 – 609)	
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	FX	Turcotte, "A Survey of Software Environments for Exploiting Networked Computing Resources," Engineering Research Center for Computational Field Simulation (June 11, 1993) (51056DOC069098 – 256)	
	FY	Vetter et al., "Network Supercomputing: Connecting Cray Supercomputers with a HIPPI Network Provides Impressively High Execution Rates," IEEE Network (May 1992) (51056DOC020930 – 936)	
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	GA	Ware et al., "64 Bit Monolithic Floating Point Processors," IEEE Journal of Solid-State Circuits, Vol. Sc-17, No. 5 (October 1982) (51056DOC059646 – 655)	
	GB	"Bit Manipulator," IBM Technical Disclosure Bulletin, pp. 1575-76 (November 1974) (51056DOC010205 - 206)	
	GC	Finney et al., "Using a Common Barrel Shifter for Operand Normalization, Operand Alignment and Operand Unpack and Pack in Floating Point," IBM Technical Disclosure Bulletin, pp. 699-701 (July 1986) (51056DOC010207 - 209)	
	GD	Data General AViiON AV500, 550, 4500 and 5500 Servers	
	GE	Jovanovic et al., "Computational Science: Advances Through Collaboration," San Diego Supercomputer Center Science Report (1993) (51056DOC068769 - 779)	
	GF	High Performance Computing and Communications: Toward a National Information Infrastructure, National Science Foundation (NSF) (1994) (51056DOC068791 - 801)	
	GG	National Coordination Office for High Performance Computing and Communications, "High Performance Computing and Communications: Foundation for America's Information Future" (1996) (51056DOC072102 – 243)	
EC	GH	Wilson, "The History of the Development of Parallel Computing," http://ei.cs.vt.edu/~history/Parallel.html (51056DOC068720 - 757)	

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EC	GI	IEEE Standard 754 (ANSI/IEEE Std. 754-1985) (51056DOC019304 - 323)	
		Original Complaint for Patent Infringement, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed March 26, 2004	
	GJ	Amended Complaint for Patent Infringement, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed April 20, 2004	
	GK	Expert Witness Report of Richard A. Killworth, Esq., *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005	
	GL	Declaration and Expert Witness Report of Ray Mercer Regarding Written Description and Enablement Issues, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005	
	GM	Corrected Expert Report of Dr. Stephen B. Wicker Regarding Invalidity of U.S. Patent Nos. 5,742,840; 5,794,060; 5,764,061; 5,809,321; 6,584,482; 6,643,765; 6,725,356 and Exhibits A-I; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 6, 2005	
	GN	Defendants Intel and Dell's Invalidity Contentions with Exhibits A-G; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 19, 2005	
	GO	Defendants Dell Inc. and Intel Corporation's Identification of Prior Art Pursuant to 35 USC §282; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 7, 2005	
	GP	Request for *Inter Partes* Reexamination Under 35 USC §§ 311-318 of U.S. Patent No. 6,725,356 filed on June 28, 2005	
	GQ	Deposition of Larry Mennemeier on September 22, 2005 and Exhibit 501; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	
	GR	Deposition of Leslie Kohn on September 22, 2005; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	
	GS	Intel Article, *"Intel Announces Record Revenue of 9.96 Billion"*, October 18, 2005	
	GT	The New York Times Article, *"Intel Posts 5% Profit Increase on Demand for Notebook Chips"*, October 19, 2005	
	GU	USA Today Article, *"Intel's Revenue Grew 18% In Robust Quarter for Tech"*, October 19, 2005	
	GV	The Wall Street Journal Article, *"Intel Says Chip Demand May Slow"*, October 19, 2005	
EC	GW	The New York Times Article, *"Intel Settlement Revives A Fading Chip Designer"*, October 20, 2005	

Examiner Signature	Eric Chan	Dated Considered	3/3/06

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. **Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450.** If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. 043876-0147	SERIAL NO. 10/705,946
	APPLICANT Craig HANSEN, et al.	
	FILING DATE November 13, 2003	GROUP 2183

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
CC	A	US	6,643,765	11-04-2003	Hansen et al.	
CC	B	US	6,725,356	04-20-2004	Hansen et al.	
		US				
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
CC	C	MARKOFF, JOHN, "Intel Settlement Revives a Fading Chip Designer," The New York Times (10-20-2005)	
CC	D	Intel Press Release, "Intel Announces Record Revenue of $9.96 Billion," Santa Clara, CA, 10-18-2005	

EXAMINER	DATE CONSIDERED
Eric Cole	3/3/06

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
43876-147	**Continuation of Application No. 10/436,340**
APPLICANT: **Craig HANSEN, et al.**	
FILING DATE: **November 13, 2003**	GROUP: **To be assigned**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Doument Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
CC		US	4,876,660	10/24/89	Owen et al.	
		US	4,956,801	09/11/90	Priem et al.	
		US	4,969,118	11/06/90	Montoye et al.	
		US	5,032,865	07/16/91	Schlunt	
		US	5,408,581	04/18/95	Suzuki et al.	
		US	5,500,811	03/19/96	Corry	
		US	5,557,724	9/17/1996	Sampat et al.	
		US	5,588,152	12/24/1996	Dapp et al.	
		US	5,640,543	6/17/1997	Farrell et al.	
		US	5,757,432	5/26/1998	Dulong et al.	
		US	5,802,336	9/1/1998	Peleg et al.	
		US	5,809,292	9/15/1998	Wilkinson et al.	
		US	5,818,739	10/6/1998	Peleg et al.	
CC		US	5,825,677	10/20/1998	Agarwal et al.	

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EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number-Kind Codes (if known)	Publication Date MYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
CC		EP 0474246 A2	9/6/1991				
CC		EP 0654733 A1	7/5/1994				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
CC		L. Kohn et al. "The Visual Instruction Set (VIS) in UltraSPARC" IEEE. 1995. 462-469.
		D. Shaver. "A General-Purpose Array Processor for Seismic Processing" (Nov - Dece 1984) January - March 1998. 15th Anniversary Issue. 5-26.
		R. Lee. "Accelerating Multimedia with Enhanced Microprocessors" IEEE Micro. April 1995. 22-32.
		N. Margulis. "i860 Microprocessor Architecture" 1990. 8-10, 171-175, 182-183.
CC		A. Levinthal et al. "Parallel Computers for Graphics Applications" 1987. 193-198.

EXAMINER: Eric Cole

DATE CONSIDERED: 3/3/06

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
43876-147	**C ntinuation f Applicati n No. 10/436,340**
APPLICANT: **Craig HANSEN, et al.**	
FILING DATE: **November 13, 2003**	GROUP: **To be assigned**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Docmen Number Number-Kind Code2 (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
EC		US 5,835,782	11/10/1998	Lin et al.	
		US 5,886,732	3/23/1999	Humpleman	
		US 5,922,066	7/13/1999	Cho et al.	
		US 5,983,257	11/9/1999	Dulong et al.	
		US 6,016,538	1/18/2000	Guttag et al.	
		US 6,092,094	7/18/2000	Ireton	
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		US 4,025,772	5/24/1977	Constant	
		US 4,489,393	12/18/1984	Kawahara, et al.	
		US 4,701,875	10/20/1987	Konishi et al.	
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		US 4,975,868	12/4/1990	Freerksen	
EC		US 5,157,388	10/20/1992	Kohn	

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EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
EC		K. Diefendorff et al. "Organization of the Motorola 88110 Superscalar RISC Microprocessor" IEEE Micro. April 1992. 40-63.	
EC		L. Gwennap. "IBM Regains Performance Lead with Power2" Microprocessor Report. October 4, 1993. Vol. 7. No. 13. 1,6-10.	
EC		L. Gwennap. "IBM Creates Power PC Processors for AS/400" Microprocessor Report. July 31, 1995. 15-16.	

EXAMINER: Eric Oh

DATE CONSIDERED: 3/3/06

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
43876-147	**C ntinuati n f Applicati n N . 10/436,340**
APPLICANT: **Craig HANSEN, et al.**	
FILING DATE: **November 13, 2003**	GROUP: **To be assigned**

U.S. PATENT DOCUMENTS

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EC		US	5,201,056	4/6/1993	Daniel et al.	
		US	5,268,855	12/7/1993	Mason et al.	
		US	5,268,995	12/7/1993	Diefendorff et al.	
		US	5,423,051	6/6/1995	Fuller et al.	
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		US	5,675,526	10/7/0997	Peleg et al.	
EC		US	5,680,338	10/21/1997	Agarwal et al.	
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